OPTIMIZATION OF BREAKDOWN VOLTAGE CHARACTERISTICS IN NORMALLY-OFF 4H-SIC VJFET USING SENTAURUS TCAD SIMULATION

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ABSTRACT*: We employ Lackner model approach to determine the temperature dependent breakdown voltage in order to improve the performance of 4H-SiC VJFET. In this letter, the maximum breakdown voltage of 14 kV is measured (drain leakage current of order of 10^{-8} A) at room temperature which corresponds to electric field of 2.1 MV/cm. It is suggested that the Lackner model for breakdown voltage simulation, which covers good fitting parameters, agrees well with the experimental and analytical reported data.*

Keywords: Breakdown voltage, electric field, leakage current, channel width, electron velocity

1. INTRODUCTION

The development and improvement of power semiconductor devices is an important task to increase the demand of high efficiency and high power density for next generation power electronic applications [1]. Silicon carbide (SiC) has unique physical and chemical properties when compared with Silicon, that make it enable for high frequency, high temperature and high voltage applications. SiC has high thermal conductivity, that means heat can easily be dissipat during high breakdown operation to achieve high voltage level [2]. High breakdown voltage is a most important advantage for SiC VJFET as compared with Si and SiC MOSFET. SiC VJFET is free of gate oxide and has no reliability issues [4]. SiC VJFET offers high breakdown voltage capability and commercially available in market. Different reports have been published during the last decades by using various analytical methods and measurements to investigate the breakdown voltage characteristics [5]. Vertical channel in JFET is a big advantage to use the complete depletion in the drift region in order to control the current and to enhance the reliability of device for high voltage switching applications [6]. A 10.4 kV normally-off trench and implanted VJFET has been designed with a drain leakage current density of 2.1 mA/cm^2 at gate voltage of V_G = 0 V [7]. However, the benefits of SiC VJFET at high temperature is likely to eliminate the cooling cost of the power system [8]. Funaki et al. reported device characteristics at temperature of 400˚C. On this regards, device has a capability to provide 500 h life time at 500˚C [9]. During the study of breakdown voltage, impact ionization is one of the important parameters on which the breakdown voltage depends, is strongly related to the distribution of electric field in the drift region [10]. Various reports related to electric field dependent impact ionization have been published using SiC Schottky barrier diode, MOSFET and BJT [11-13]. Furthermore, punch through behavior has also been examined in SiC PiN diode [14]. To the best of our knowledge variation in electric field with punch through behavor reported first time using SiC VJFET. In this paper, 2D numerical simulations of normally-off 4H-SiC VJFET are studied in detail. The effect of temperature and negative gate bias on the breakdown voltage analysis is presented. Punch through behavior was examined through finite element simulations.

2. DEVICE STRUCTURE

Fig. 1 shows the cross-sectional view of the proposed structure of SiC VJFET. In order to achieve desirable properties of a device it should be necessary to precisely consider the design parameters. The parameters focused for this structure are drift layer thickness along with doping concentration and channel width. It has been observed that the breakdown voltage is mainly governed by the thickness of the drift layer and low drift doping as well. However, the proposed structure of SiC VJFET consist of: a 120 µm drift layer with lightly drift doped of N_D = 6.4 x 10^{14} cm^{-3}, a channel width accomplished by adjusting the separation of two gates which is selected to be 1.0 µm, and the doping of channel region is 4 x 10^{15} cm^{-3} which is very essential for the requirement of normally-off behavior. The other selected parameters and experimental procedure is available in [7, 15]. It is also clear from figure that the device has unconstructed mesh arranged around the channel. The purpose of meshing needs to describe the approximate numerical solution. Although unconstructed mesh is very difficult to create but is more realize than constructed mesh. Generally, we need dense mesh where the carrier concentration and, electric field has high gradient.

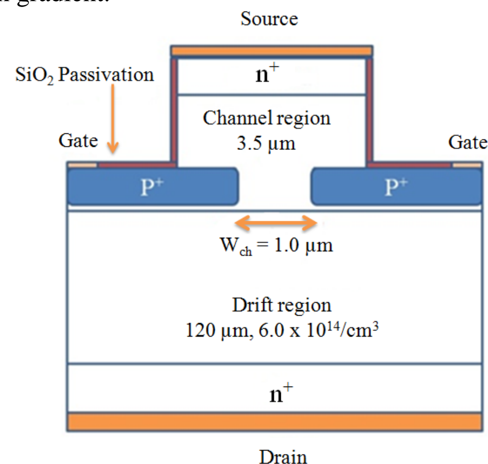

Figure 1. Simplified cross-sectional view of 14 kV normally-off 4H-SiC VJFET.

3. MODEL APPROACH

In this simulation, model could not be fitted exactly but it is possible to measure the breakdown voltage that well

correlated with the published literature. To the best of our knowledge the Lackner model used first time for the simulation of SiC VJFET. However, the expression for the total generation rate is given by

$$G^{ii} = \alpha_n n v_n + \alpha_p p v_p \quad (1)$$

Where α_n and is an impact ionization coefficient and would be modelled by Lackner [16] given by the following equation

$$\alpha_{n,p}(F_{ava}) = \frac{\gamma a_{n,p}}{z} \exp(-\frac{\gamma b_{n,p}}{F_{ava}}) \quad (2)$$

$$z = 1 + \frac{\gamma b_n}{F_{ava}} \exp\left(-\frac{\gamma b_n}{F_{ava}}\right) + \frac{\gamma b_p}{F_{ava}} \exp\left(-\frac{\gamma b_p}{F_{ava}}\right) \quad (3)$$

$$\gamma = \frac{\tanh(\frac{\hbar\omega_{op}}{2KT_0})}{\tanh(\frac{\hbar\omega_{op}}{2KT})} \quad (4)$$

In the above equations, $\hbar\omega_{op}$ represents the optical phonon energy and F_{ava} represents the magnitude of electric field. Akturk et al. [17] reported that a_n and a_p are the multiplicative coefficients varies linearly with temperature [18]. While b_n and b_p are the critical field for both electrons and holes, and γ is a constant value. These fitting parameters are summarized in table 1.

Table 1: Impact ionization fitting parameters used for simulation

Parameter	a (cm^{-1})	b (V/cm)	γ
Electron	2.10 x 10^7	1.70 x 10^7	1
Hole	2.96 x 10^7	1.60 x 10^7	1

4. RESULTS AND DISCUSSION

In order to investigate the breakdown voltage analysis, Fig. 2 (a) shows the negative gate bias dependent breakdown voltage characteristics at room temperature. It is clear that high negative gate voltage has actually resulted in a high breakdown voltage. The device exhibits limited breakdown voltage capability and no such significant behaviour was observed at $V_G \leq -5$ V. Thus, holes collected at gate with more negative bias substantially decrease the drain leakage current. The minimum leakage current at $V_G = -5$ V was observed 2.66 x 10^{-8} A, leading to a reduction which is approximately one order of magnitude lower than when compared with zero gate bias. It has been reported that high negative voltage is most likely needed for wider channel opening [19]. The device in [15], had channel width of 0.77 µm, which has zero gate bias to achieve breakdown voltage of 14 kV. In our simulation case, for channel width of 1.0 µm requires a gate voltage of -5 V to achieve breakdown voltage of 14 KV which leads to a 33% higher than by experimental value reported by [20] but slightly 9 % lower than the theoretical value reported by [7]. It is worth noting that almost identical breakdown voltage reported by Zaho et al. [15] at $V_G = 0$ V has good agreement with the present simulation results.

Fig. 3 shows the observed decrease in breakdown voltages with increasing temperature is well agreement reported by Veliadis et al. [21]. When temperature increases from 25 to 500˚C, breakdown voltage decreases from 14 to 9.0 kV. The device exhibits negative temperature coefficient for breakdown voltage which can be attributed to the reduction of a depletion region due to generation of charge carriers. This allowed leakage current increases from 2.1 x 10^{-7} to 3.6 x 10^{-7} A. However, very little information available related to temperature dependent breakdown voltage in 4H-SiC VJFET.

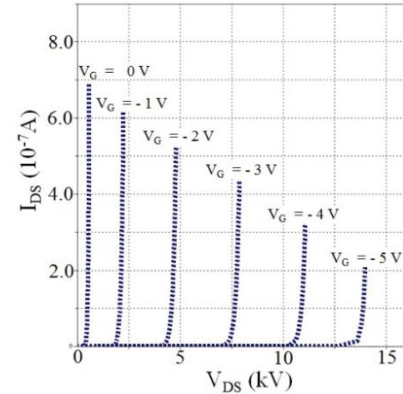

Figure 2: Simulated breakdown characteristics with the dependence of negative gate bias from -5 to 0 V. The breakdown voltage of 573 V at 0 gate bias is clear indication of normally-off behavior.

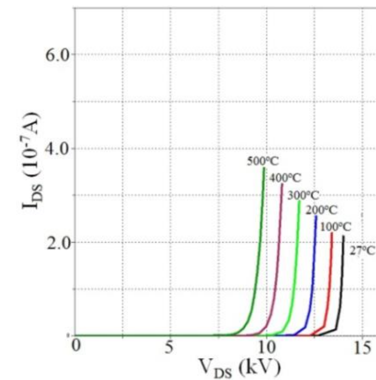

Figure 3: Simulation of temperature dependence breakdown voltage in the temperature ranges from 25 to 500˚C.

Temperature dependent electric field measurement was performed which provides complete conclusive evidence that the electric field is responsible for the breakdown voltage. Since breakdown voltage is related to the strength of electric field, increasing the electric field strength will help to increase the breakdown voltage. Simulation results indicate the temperature dependent electric field spreading effect at $V_G = -5$ V in the device depth as shown in Fig. 4. There is indeed large electric field distribution start strongly at the edge of the gate and decreases away from the gate to drain side as clear in Fig. 4 (a). Since surface is covered by SiO_2 passivation layer. Therefore, electric field at the surface is negligible to consider. 2D grid confirms the strong electric field distribution at the edge of gate as clear in Fig. 4 (b, c). It is found that closed contour vertical lines represent the transverse electric field while broad lines represent the longitudinal electric field. It has been observed from Fig. 4

(a) that the overshoot in an electric field is responsible due to strength of longitudinal field. Here, electric filed approach to a maximum value of 2.1 MV/cm which was measured at room temperature. At temperature of 500˚C, approximately 16.6 % reduction in electric field was observed when compared with the value obtained at room temperature. The punch through is an important parameter for obtaining high breakdown voltage. The factors that affect on the punch through were taken into account such as low drift doping and low channel width. In ideal case, the behaviour of the electric field is like triangular. The punch through has three layer structure n^- -p^+ -n^- in which n^- -p^+ is formed by the channel and gate junction whereas, p^+ -n^- is formed by the gate drift junction. It is found that the doping in the channel is one order of magnitude higher than that of drift doping. Therefore, p^+ -n^- is more significant in order to activate punch through behaviour. If the doping of drift region is higher or equal to the channel doping, the breakdown voltage occurs before the punch through. Here, doping is lower in channel region, therefore punch through voltage occurs before in which most of the breakdown voltage occurs utilizing the full drift layer. It is found that the depletion should be extend more, but high drain doping limits the depletion region consequently enhance the punch through voltage. It is clear from figure that this behaviour remains relatively observed at high temperature. We fine the electric field at the interface of drift and drain measured 0.44 and 0.15 MV/cm corresponding to the 21 % and 8.5.% of the critical field at room and high temperature, respectivrly.

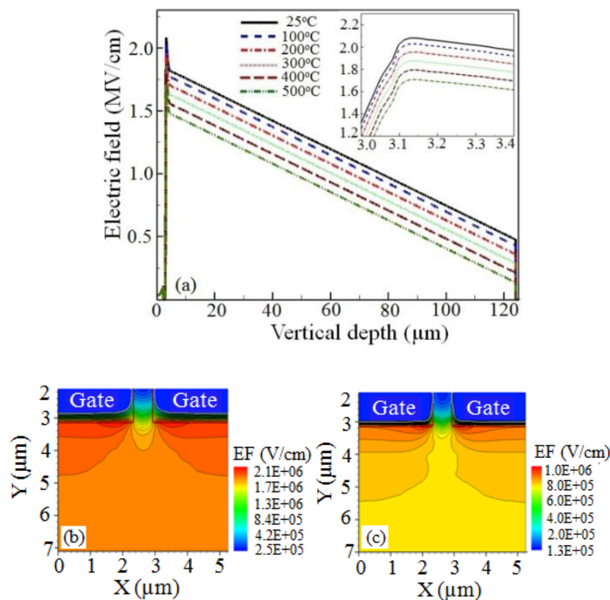

Figure 4. (a) Vertical depth dependence electric field distribution with the influence of temperature from 25 to 500˚C. Image diagram which shows the 2D distribution of the electric field at temperature of (b) 25˚C (c) 500˚C

Fig.5 shows the electron velocity as a dependence of vertical depth obtained at different temperatures. We note that the electron velocity initially increases due to influence of high electric field as clear at point 1. The overshoot in velocity is due to high longitudinal electric field observed in Fig 4. The overshoot in velocity has been investigated by Maia et al. [22] showed the saturation velocity was observed by the effect of high electric field. In case of high temperature, increase in the large number of intrinsic carriers minimized the effect of electric field, which results in the reduction of electron velocity. Specifically, the average electron saturation velocity at room temperature is 4.4 x 10^7 cm/s under high electric field of 2.1 MV/cm; this value decreases at 500˚C and reaches approximately 1.6 x 10^7 at 1.8 MV/cm. In addition, electron undergoes very significant scattering near the gate in the drift region for a small distance shown at point 2. Therefore, there is a little deviation in electron velocity was observed. The actual reason for this deviation is the superimposing of transverse and longitudinal electric field near the gate. It is worth noting that constant velocity in drift region is governed by the compensation of both electric fields which is due to the constant drift doping profile as clear by point 3.

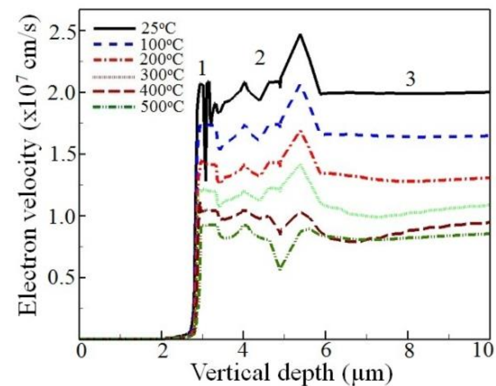

Figure 5: Vertical depth dependence electron velocity affected by temperature.

5. CONCLUSION

In conclusion, for the normally-off 4H-SiC VJFET, we have proposed breakdown voltage of (14 kV) which corresponds to extremely low leakage current of the order of 10^{-8} A. Furthermore, it has been demonstrated that the device structure has shown the negative temperature coefficient for breakdown voltage. In addition, simulation analysis shows that carrier generation process at room temperature is more dominant under high negative bias. Herein, we have theoretically reported the presence of punch through behavior at high negative gate bias for the first time. To the best of our knowledge, these observations are not yet discussed experimentally. These investigations will definitely help to improve the functionality of experimentally designed devices afterwards. Finally, we suggest that the Lackner is a predictive model for the analysis of temperature dependent breakdown voltage characteristics of 4H-SiC VJFET.

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